

# MRTL

## INTEGRATED CIRCUITS

# mW MRTL

MC800 Series (0 to +75°C)

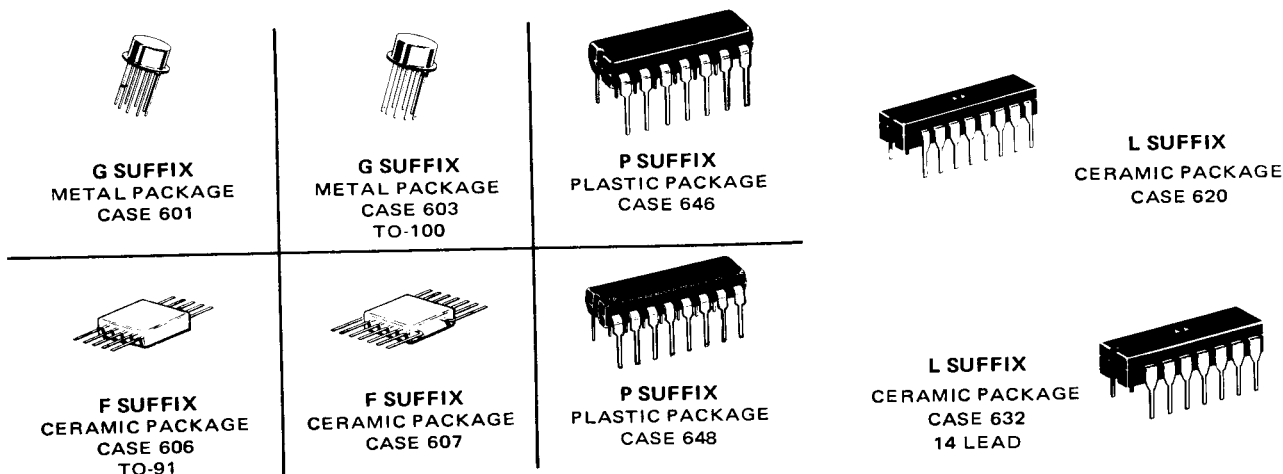
MC900 Series (-55 to +125°C)

### NEW MRTL AND mW MRTL

The new MRTL and mW MRTL 800 Series described in this selector guide are now designed to exceed both the old MC700 and the old MC800 Series electrical characteristics. This has been accomplished by combining the critical electrical parameters of both the MC700 and MC800 Series into one standard series, the new MC800 Series.

Medium-power MRTL integrated circuits provide a broad line of low-cost, multi-function, digital circuits. Typical gate speed is 12 ns, with power dissipation averages of 19 mW (input high) and 5.0 mW (inputs low) per logic node. Devices from the MC800 Series have loading factors normalized for compatibility with the low-power mW MRTL devices for ease in mixing the two power levels in a system.

Low-power mW MRTL integrated circuits are designed for use where minimal system power consumption is desired. Typical gate speed is 27 ns, with typical power dissipation of 6.5 mW (input high) and 0.5 mW (inputs low) per logic node. Devices from the mW MRTL Series can be mixed with devices from the medium-power MRTL Series which has loading factors normalized for compatibility.



Functions	MRTL	mW MRTL	Type 1 MC800 Series 0 to +75°C	MC800 Series Case	Type 1 MC900 Series -55 to +125°C	MC900 Series Case	Loading Factors Each Output			tp ns typ	Power Dissipation	
							MRTL With mW MRTL	MRTL With MRTL	mW MRTL With mW MRTL		MC800 P&L Series	MC900 F&G Series
Buffer	*				MC900	601,606	80	25	-	20		16/45 2
Counter Adapter	*				MC901	601,606	16	5	-	22		55
R.S. Flip-Flop	*				MC902	601,606	13	4	-	14		22
3-Input NOR Gate	*				MC903	601,606	16	5	-	12		19/5 2
Half Adder	*				MC904	601,606	16	5	-	14		45
Half-Shift Register	*				MC905	601,606	13	4	-	22		53
Half-Shift Register (w/o Inverter)	*				MC906	601,606	13	4	-	22		36
4-Input NOR Gate	*				MC907	601,606	16	5	-	12		19/5 2
Half-Adder	*	*			MC908	601,606	-	-	4	60		14/8 5 2
2-Input Buffer	*	*			MC909	601,606	-	-	30	57		5.5/16 2
Dual 3-Input (NOR Gate)	*	*			MC910	601,606	-	-	4	27		8.0/1.0 2
4-Input OR/NOR Gate	*	*			MC911	601,606	-	-	4	60		6.0/3 5 2
Half-Adder	*	*			MC912	601,606	-	-	4	66		11.5/5 5 2
Type D-Flip-Flop	*	*			MC913	601,606	-	-	3	75		17.5/13 5
Dual 2-Input NOR Gate	*	*			MC914	601,606	16	5	-	12		38/10 2
Dual 3-Input NOR Gate	*	*	MC815	646,632	MC915	603,606	16	5	-	12	55/15 2	38.10 2
J.K. Flip-Flop	*	*	MC816	646,632	MC916	601,606	10	3	-	30	91/79 3	62 54 3
Quad 2-Input NOR Gate	*	*	MC817	646,632	MC917	607	-	-	4	27	20/5.0 2	16.2 5 2
Dual 3-Input NOR Gate	*	*	MC818	646,632	MC918	603,606	-	-	4	27	12/2.5 2	9.5 1.0 2
Dual 4-Input NOR Gate	*	*	MC819	646,632	MC919	607	-	-	4	27	13/2.5 2	11 1.0 2
J.K. Flip-Flop	*	*			MC920	601,606	-	-	2	50		15 5 10 3
Dual 2-Input Gate Expander	*	*			MC921	601,606	-	-	-	27		3 0 - 2
J.K. Flip-Flop	*	*			MC922	603,606	-	-	4	70	24/20 3	17.5 13 3
Quad 2-Input NOR Gate	*	*	MC822	646,632	MC924	607	16	5	-	12	100/30 2	76 2C 2
Dual 4-Input NOR Gate	*	*	MC825	646,632	MC925	607	16	5	-	12	60/15 2	36 1C 2

Functions	MRTL	mW MRTL	Type 1 MC800 Series 0 to +75°C	MC800 Series Case	Type 1 MC900 Series -125 to +125°C	MC900 Series Case	Loading Factors Each Output			tp ns typ	Power		Dissipation	
							MRTL With mW MRTL	MRTL With MRTL	mW MRTL With mW MRTL		MC800 P&L Series	MC900 F&G Series		
J.K. Flip-Flop Wuad Inverter 5-Input NOR Gate 5-Input NOR Gate Dual Exclusive (OR/NOR Gate)	*	*	MC826	646,632	MC926 MC927 MC928 MC929	603,606 603,606 601,606 601,606	16 16 — 16	5 5 — 5	— — 4 —	35 12 27 12	100/86 3	130/65 3 76/20 2 6.5/0.5 2 19/5 2		
Quad Latch BCD to Decimal Decoder Quad Exclusive OR Gate J.K. Flip-Flop Dual Half-Adder	*	*	MC867,A MC870 MC871	648,620 648,620 646,632	— — MC971 MC974 MC975	— — 607 601,606 607	— — 16 16 16	— — 5 5 5	— — — — 2	— 9 7 12 35 20	25 110 100/— 72	— — 28 130/65 3 90		
Dual J.K. Flip-Flop Binary Up Counter Dual Type D Flip-Flop 1 J.K. Flip-Flop, 1 (Expander, 2 Buffers)	*	*	MC876 MC877 MC878 MC879	646,632 646,632 646,632 646,632	MC976 — MC978 —	607 — 607 —	— — 10 —	— — 3 —	— — — 3	50 — 60 —	41/29 3 180 48/35 5 141/124 4	31/20 3 — 35/26 5 —		
Decade Up Counter Dual Buffer J.K. Flip-Flop Dual Half-Shift Register Dual Half-Shift Register (w/Inverter)	*	*	MC880 — — MC883 MC884	646,632 — — 646,632 646,632	— MC891 MC892 MC893 MC894	— 601,606 601,606 607 607	10 — — 13 13	3 — — 4 4	— — — — —	— 57 80 22 22	250 — — 140 100	— 11/32 2 15/13 3 110 75		
Quad 2-Input Expander Dual 4-Input Expander 1 J.K. Flip-Flop, 1 Inverter (2, Buffers) Dual 3-Input Buffer (Non-Inverting) Hex Inverter	*	*	MC885,A MC886 — MC887 MC888 MC889,A	646,632 646,632 — 646,632 646,632 646,632	MC985 MC986 — — MC988 MC989	607 607 — — 607 607	— — — — 80 16	— — — — 25 5	— — — — — —	12 12 — — 24 12	20/— 2 20/— 2 — — 138/132 4 145/56 2 130/15 2	17/— 2 17/— 2 — — 124/42 2 76/20 2		
Dual J.K. Flip-Flop Dual J.K. Flip-Flop Triple 3-Input NOR Gate Triple 3-Input NOR Gate Serial-Parallel Shift Register	*	*	MC890 MC891 MC892 MC893 MC894	646,632 646,632 646,632 646,632 646,632	MC990 MC991 MC992 MC993 —	607 607 607 607 —	10 16 16 16 16	3 5 5 — 5	— — — 4 —	35 40 12 27 55	182/158 3 190/160 3 82/24 2 18/3.5 2 225	124/108 3 155/130 3 57/15 2 14/2.0 2 —		
Dual Full Adder Dual Full Subtractor Dual 2-Input Buffer Dual Buffer Dual 4-Channel (Data Selector)	*	*	MC896 MC897 MC898 MC899 MC9801	646,632 646,632 646,632 646,632 648,620	MC996 MC997 MC998 MC999 —	607 607 607 603, 606 —	16 16 80 80 16	5 5 — 25 5	— — 30 — —	60 60 57 15 25	225 225 14/46 2 50/90 2 100	190 190 11/32 2 32/90 2 —		
Dual J.K. Flip-Flop 4-Bit Parallel Full Adder Dual 4-Channel (Data Distributor) Quad Schmitt Trigger Quad 2-Input AND Gate	*	*	MC9802 MC9804 — MC9807 MC9809 MC9813	646,632 648,620 — 648,620 646,632 646,632	— — — — — —	— — — — — —	10 6 — 16 16 16	3 2 — 5 5 5	— — — — — —	35 125 — 25 30 28	182/158 3 265 — 150 95 100	— — — — — —		
Quad 2-Input NAND Gate Quad 2-Input OR Gate Hex Inverter Hex Expander Hex Expander	*	*	MC9814 MC9815 MC9818 MC9819,A MC9820	646,632 646,632 646,632 646,632 646,632	— — — — —	— — — — —	16 16 — — —	5 5 — — —	— — 4 — —	35 40 27 12 12	145 28/100 2 7.0/3.0 2 13/— 2 30/— 2	— — — — —		
Quad 2-Input Expander Dual J.K. Flip-Flop Quad 2-Input AND Gate Quad 2-Input NAND Gate Quad 2-Input OR Gate	*	*	MC9821 MC9822 MC9823 MC9824 MC9825	646,632 646,632 646,632 646,632 646,632	— — — — —	— — — — —	— — — — —	— — — 4 4 4	— — — — —	27 75 50 50 50	20/— 2 24/— 3 12 6 20/5.0 2 -7.0 2	— — — — —		

"A" Suffix devices have insured capability to drive at least one M TTL load or two M DTL loads.

- 1 G suffix denotes Metal, F suffix Flat Package, P suffix denotes Plastic Package, L suffix denotes dual inline Ceramic Package.
- 2 Inputs High/Inputs Low unless otherwise noted.
- 3 Only clock inputs High/Input Low.
- 4 Only clock inputs high on Flip-Flop, other elements High/Inputs Low.
- 5 Direct Set & Direct Clear Low, all other inputs high/all inputs low.
- 6 One input high/one input low.

$V_{CC} = 3.0V \pm 10\%$  for MC900 Series devices.

$V_{CC} = 3.6V \pm 10\%$  for MC800 Series devices.

Power Dissipation and  $t_p$  typicals at  $T_A = 25$

# INSTRUCTIONS FOR USE OF PACKAGE INFORMATION TABLE

MC900 and MC800 Series Low-Power mW MRTL devices are available in the packages pictured in the following table as indicated on the line following each device type number. Plastic packaged devices are available in the MC800 Series only.

- Pin numbers for any of the following devices and packages may be determined by:
- Locate the device as shown in the logic diagrams appearing on the preceding pages (grouped by function). Note the alpha pin designations for the device.
  - Find the device type number in the left hand columns of the "Package Information Table".
  - The letters in the columns following the type number and below the drawing of the desired package indicate the correct pin numbers for the specific package by their numbered positions beneath the package drawing. (These letters are the same as indicated on the logic diagram for the device.)
  - Notes: Blanks in an area following the type number and directly beneath a package indicate the device is not available in that package. A dash indicates this pin or lead is not connected nor otherwise utilized for this device and package. \* indicates this pin number is the ground connection for this device and package. # indicates this pin number is the V<sub>CC</sub> connection for this device and package.

## PACKAGE INFORMATION TABLE

		L OR P SUFFIX CERAMIC & PLASTIC PACKAGES															F SUFFIX CERAMIC PACKAGES														G SUFFIX METAL PACKAGES														
Type No.	Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1	2	3	4	5	6	7	8	9	10				
	MC908																																												
	MC909																																												
	MC910																																												
	MC911																																												
	MC912																																												
	MC913																																												
	MC817	MC917	a	b	c	*	e	f	g	h	i	j	=	l	m	n		a	b	c	f	g	e	*	h	i	j	n	l	m	#														
	MC818	MC918	-	b	c	*	e	f	-	-	i	j	=	l	m	-		b	l	m	e	*	f	i	j	c	=																		
	MC819	MC919	-	b	c	*	e	f	g	-	i	j	=	l	m	n		l	b	c	-	m	n	*	e	f	g	-	i	j	#														
	MC920																																												
	MC921																																												
	MC822	MC922	-	b	c	*	-	f	-	-	i	j	=	l	m	-		l	m	b	c	*	-	f	i	j	#																		
	MC928																																												
	MC864	-	a	b	c	*	e	f	g	h	i	j	=	l	m	n																													
	MC867	-	a	b	c	*	e	f	g	h	i	j	k	-	n	p	q																												
	MC870	-	a	b	c	*	e	f	g	h	i	j	k	l	=	n	p	q																											
	MC876	MC976	a	b	c	*	e	f	g	h	i	j	=	l	m	n		l	m	n	a	b	c	*	e	f	g	h	i	j	#														
	MC878	MC978	a	b	c	*	e	f	g	h	i	j	=	l	m	n		l	m	n	a	b	c	*	e	f	g	h	i	j	#														
	MC981																																												
	MC982																																												
	MC893	MC993	a	b	c	*	e	f	g	h	i	j	=	l	m	n		a	b	f	g	h	e	*	i	j	l	m	c	n	#														
	MC898	MC998	-	b	c	*	e	f	-	-	i	j	=	l	m	-		l	m	-	-	b	c	*	e	j	-	-	i	f	#														
	MC9818	-	a	b	c	*	e	f	g	h	i	j	=	l	m	n																													
	MC9820	-	a	b	c	*	e	f	g	h	i	j	=	l	m	n																													
	MC9821	-	a	b	c	*	e	f	g	h	i	j	=	l	m	n																													
	MC9822	-	a	b	c	*	e	f	g	h	i	j	=	l	m	n																													
	MC9823	-	a	b	c	*	e	f	g	h	i	j	#	l	m	n																													
	MC9824	-	a	b	c	*	e	f	g	h	i	j	#	l	m	n																													
	MC9825	-	a	b	c	*	e	f	g	h	i	j	#	l	m	n																													

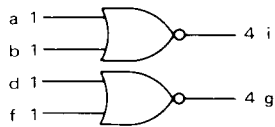
### MAXIMUM RATINGS (T<sub>A</sub> = +25°C)

Rating	Symbol	Value	Unit
Input Voltage	-	±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 second)	-	+6	Vdc
Operating Temperature Range MC900 Series MC800 Series	T <sub>A</sub>	-55 to +125 0 to +75	°C
Storage Temperature Range Metal Packages, Flat Packages Plastic Packages	T <sub>stg</sub>	-65 to +150 -55 to +125	°C

The numbers at the end of the terminals indicate loading factors for low-power mW MRTL devices. Pin numbers vary with the package types. The alpha pin designations shown on the logic diagrams, used in conjunction with the Package Information Table (following the logic diagrams), make it possible to ascertain pin numbers for a specific device and package.

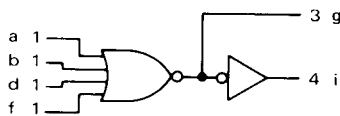
## GATES

**MC910**  
Dual 2-Input NOR Gate



$$i = \overline{a + b}$$

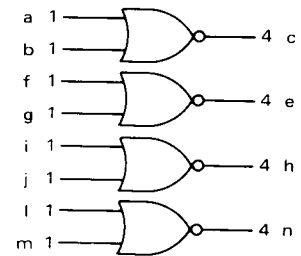
**MC911**  
4-Input OR/NOR Gate



$$g = \overline{a + b + d + f}$$

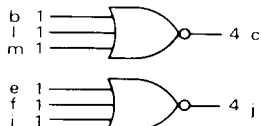
$$i = a + b + d + f$$

**MC817, MC917**  
Quad 2-Input NOR Gate



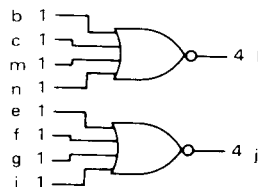
$$c = \overline{a + b}$$

**MC818, MC918**  
Dual 3-Input NOR Gate



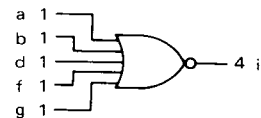
$$c = \overline{b + l + m}$$

**MC819, MC919**  
Dual 4-Input NOR Gate



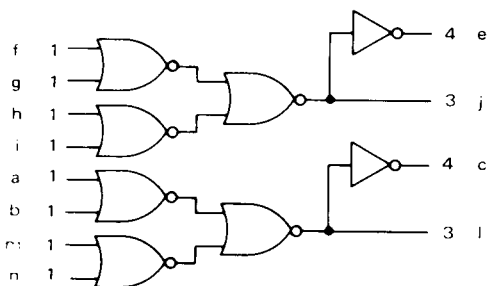
$$l = \overline{b + c + m + n}$$

**MC928**  
5-Input NOR Gate



$$i = \overline{a + b + d + f + g}$$

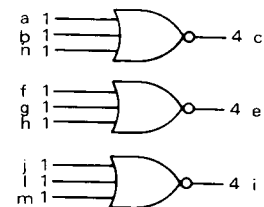
**MC864**  
Dual Exclusive OR-NOR Gate



$$l = (a + b) \cdot (m + n)$$

$$c = \overline{a \cdot b + m \cdot n}$$

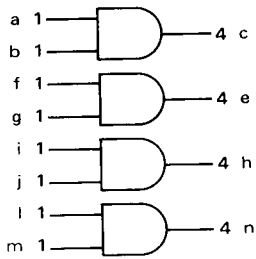
**MC893, MC993**  
Triple 3-Input NOR Gate



$$c = \overline{a + b + n}$$

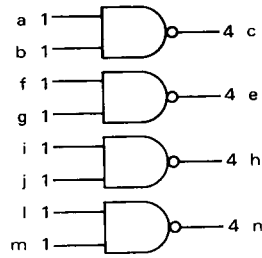
## GATES (continued)

**MC9823**  
Quad 2-Input AND Gate



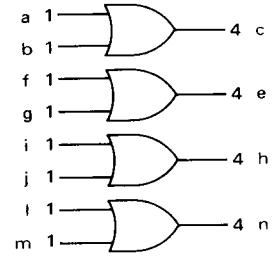
$$c = a \cdot b$$

**MC9824**  
Quad 2-Input NAND Gate



$$c = \overline{a \cdot b}$$

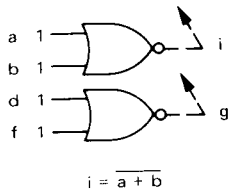
**MC9825**  
Quad 2-Input OR Gate



$$c = a + b$$

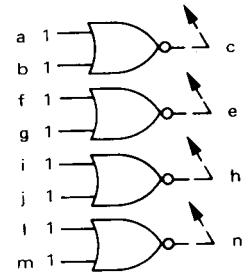
## EXPANDERS

**MC921**  
Dual 2-Input Expander



$$i = \overline{a + b}$$

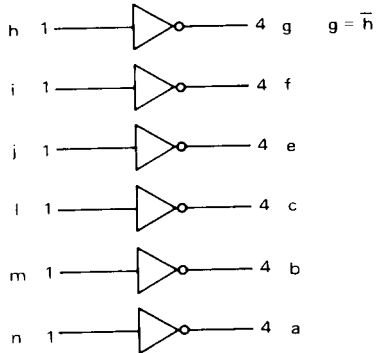
**MC9821**  
Quad 2-Input Expander



$$c = \overline{a + b}$$

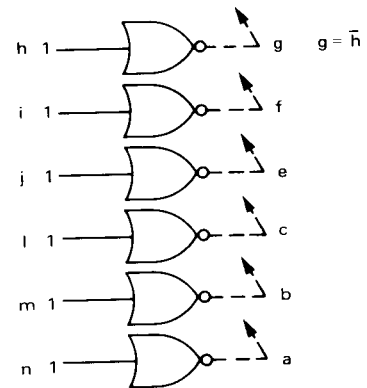
## INVERTER

**MC9818**  
Hex Inverter



$$g = \bar{h}$$

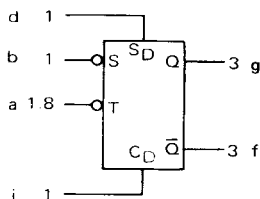
**MC9820**  
Hex Expander



$$g = \bar{h}$$

FLIP-FLOPS

MC913  
Type D Flip-Flop



DIRECT INPUT OPERATION ①

S <sub>D</sub>	C <sub>D</sub>	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

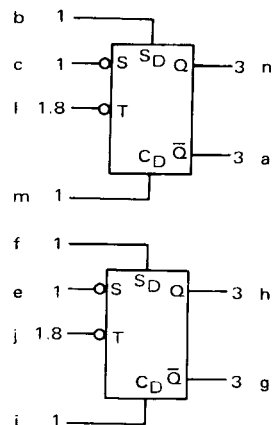
t <sub>n</sub>	t <sub>n+1</sub>	S	Q	$\bar{Q}$
		1	1	0
		0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from S<sub>D</sub> = C<sub>D</sub> to S<sub>D</sub> = C<sub>D</sub> = 0. The output state cannot be predetermined in the case where the input goes from S<sub>D</sub> = C<sub>D</sub> = 1 to S<sub>D</sub> = C<sub>D</sub> = 0.
3. Direct inputs (S<sub>D</sub> and C<sub>D</sub>) must be low.

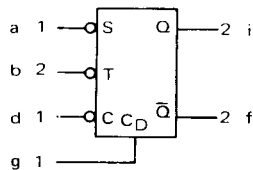
0 = low state  
1 = high state

t<sub>n</sub> = time period prior to negative transition of clock pulse  
t<sub>n+1</sub> = time period subsequent to negative transition of clock pulse

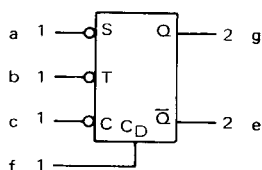
MC878, MC978  
Dual Type D Flip-Flop



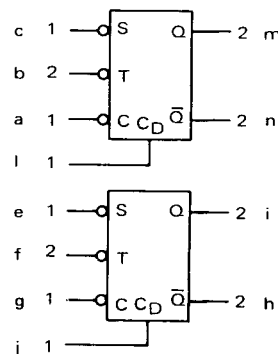
MC920  
J-K Flip-Flop



MC982  
J-K Flip-Flop



MC876, MC976  
Dual J-K Flip-Flop



CLOCKED INPUT OPERATION

t <sub>n</sub>	t <sub>n+1</sub>	S	C	Q <sub>n</sub>	$\bar{Q}_n$	Q <sub>n+1</sub>	$\bar{Q}_{n+1}$
		1	1	Q <sub>n</sub>	$\bar{Q}_n$	0	0
		1	0	1	0	0	1
		0	1	0	1	0	1
		0	0	$\bar{Q}_n$	Q <sub>n</sub>	0	0

Direct input (C<sub>D</sub>) must be low.

0 = low state  
1 = high state

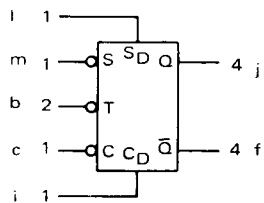
t<sub>n</sub> = time period prior to negative transition of clock pulse.

t<sub>n+1</sub> = time period subsequent to negative transition of clock pulse.

Q<sub>n</sub> = state of Q output in time period t<sub>n</sub>.

NOTE:  
Clock pulse fall time must be within the range of 10 ns to 100 ns on all J-K Flip-Flops.

MC822, MC922  
J-K Flip-Flop



DIRECT INPUT OPERATION ①

S <sub>D</sub>	C <sub>D</sub>	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t <sub>n</sub>	t <sub>n+1</sub>	S	C	Q	$\bar{Q}$
		1	1	Q <sub>n</sub>	$\bar{Q}_n$
		1	0	1	0
		0	1	0	1
		0	0	$\bar{Q}_n$	Q <sub>n</sub>

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from S<sub>D</sub> = C<sub>D</sub> to S<sub>D</sub> = C<sub>D</sub> = 0. The output state cannot be predetermined in the case where the input goes from S<sub>D</sub> = C<sub>D</sub> = 1 to S<sub>D</sub> = C<sub>D</sub> = 0.
3. Direct inputs (S<sub>D</sub> and C<sub>D</sub>) must be low.

0 = low state  
1 = high state

t<sub>n</sub> = time period prior to negative transition of clock pulse  
t<sub>n+1</sub> = time period subsequent to negative transition of clock pulse

Q<sub>n</sub> = state of Q output in time period t<sub>n</sub>

(continued)

## FLIP-FLOPS (continued)

### MC867 Quad Latch

**TRUTH TABLE**

E	D	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
0	0	Q <sub>n</sub>	Q̄ <sub>n</sub>
0	1	Q <sub>n</sub>	Q̄ <sub>n</sub>
1	0	0	1
1	1	1	0

### MC9822 Dual J-K Flip-Flop

**CLOCKED INPUT OPERATION ①**

t <sub>n</sub> ②		t <sub>n+1</sub> ②	
S	C	Q	Q̄
1	1	Q <sub>n</sub> ③	Q̄ <sub>n</sub>
1	0	1	0
0	1	0	1
0	0	Q̄ <sub>n</sub>	Q <sub>n</sub> ③

1. Direct input (C<sub>D</sub>) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t<sub>n</sub> and the time period subsequent to this transition is denoted t<sub>n+1</sub>.
3. Q<sub>n</sub> is the state of the Q output in the time period t<sub>n</sub>.

## HALF ADDERS

### MC908 Half Adder

$$i = (a + b)(\bar{d} + \bar{f})$$

$$g = \bar{d} + \bar{f}$$

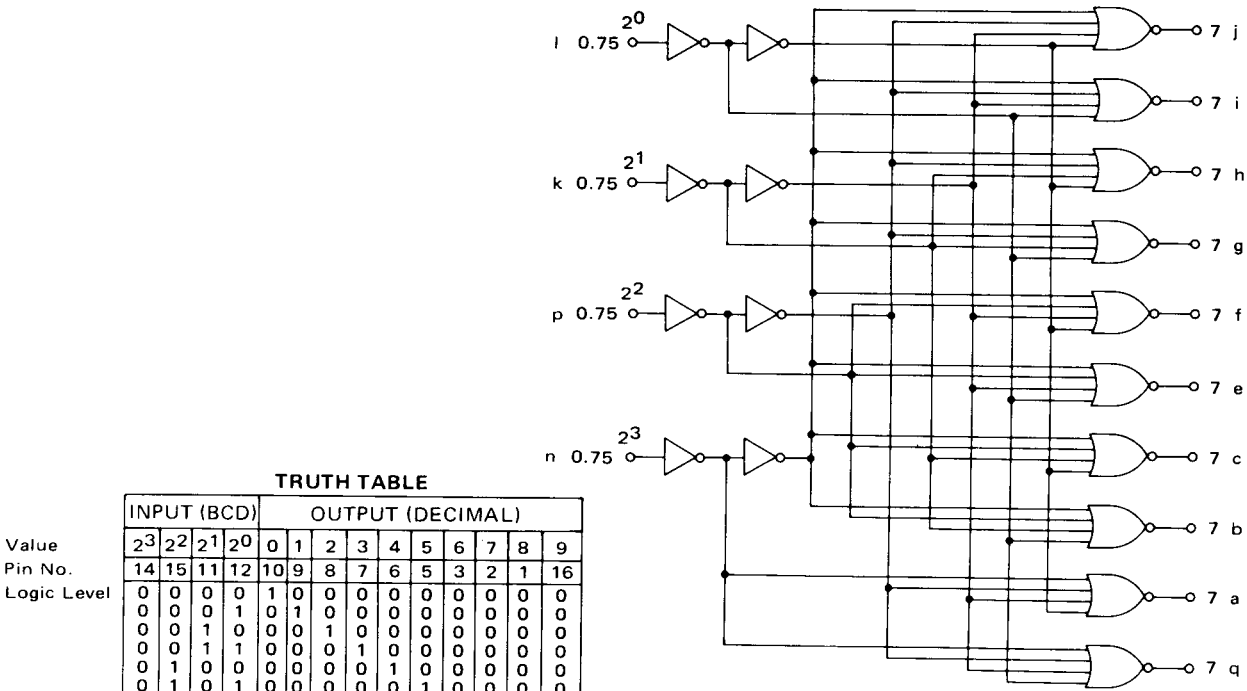
### MC912 Half Adder

$$g = \bar{a} \cdot \bar{b} + \bar{d} \cdot \bar{f}$$

$$i = (a + b)(d + f)$$

**DECODER**

**MC870  
BCD-to-Decimal Decoder**

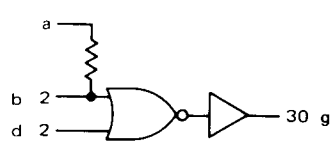


**TRUTH TABLE**

Value Pin No. Logic Level	INPUT (BCD)				OUTPUT (DECIMAL)										
	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>	0	1	2	3	4	5	6	7	8	9	16
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

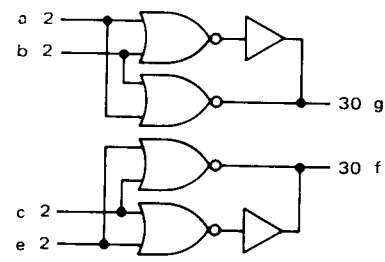
**BUFFERS**

**MC909  
Buffer**



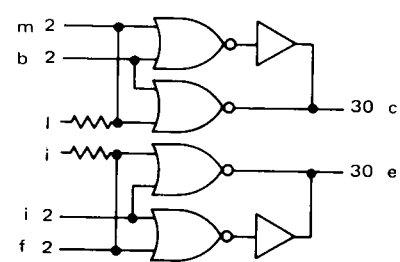
$g = \overline{b + d}$

**MC981  
Dual Buffers**



$g = \overline{a + b}$

**MC898, MC998  
Dual Buffers**



$c = \overline{b + m}$

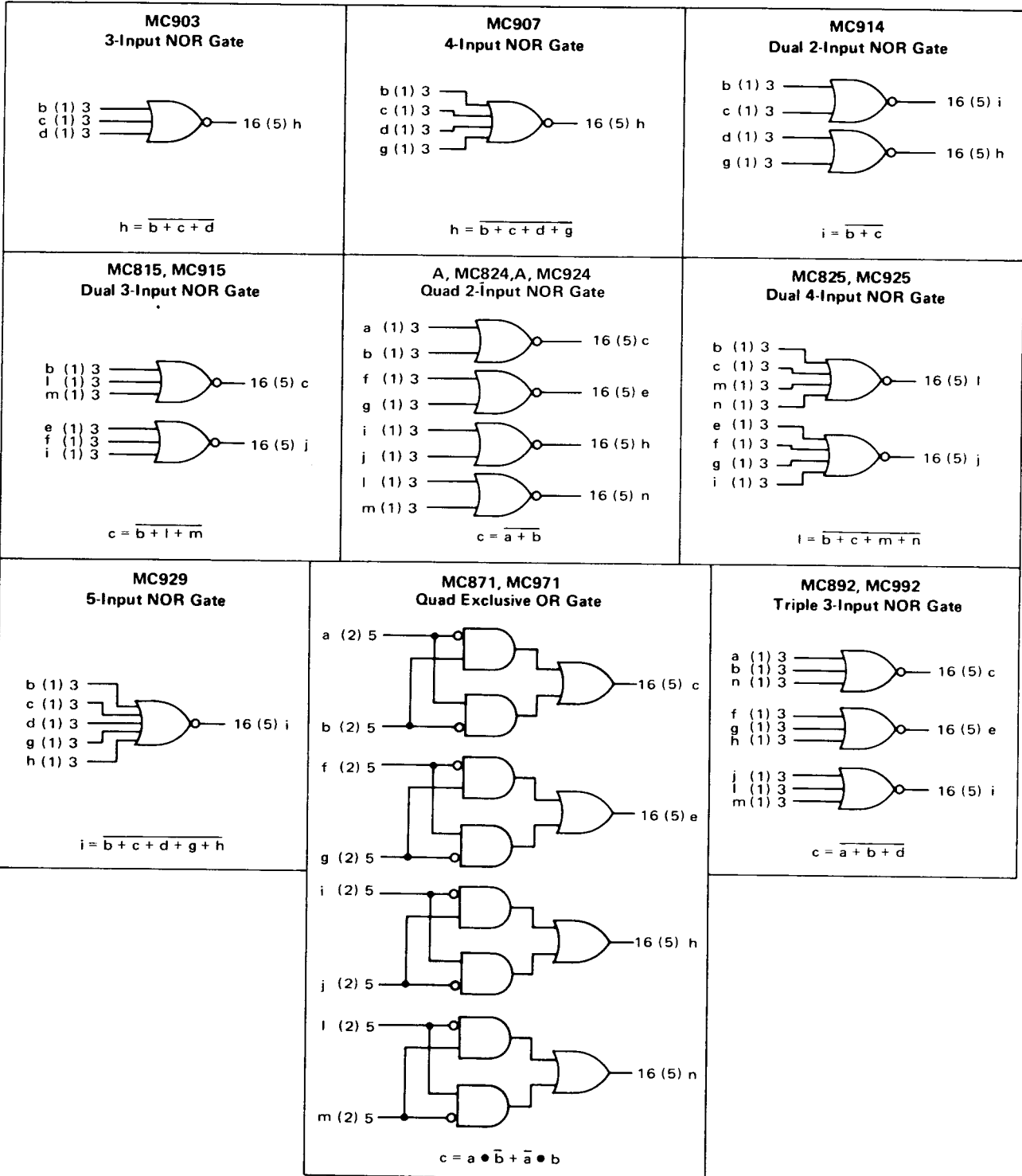




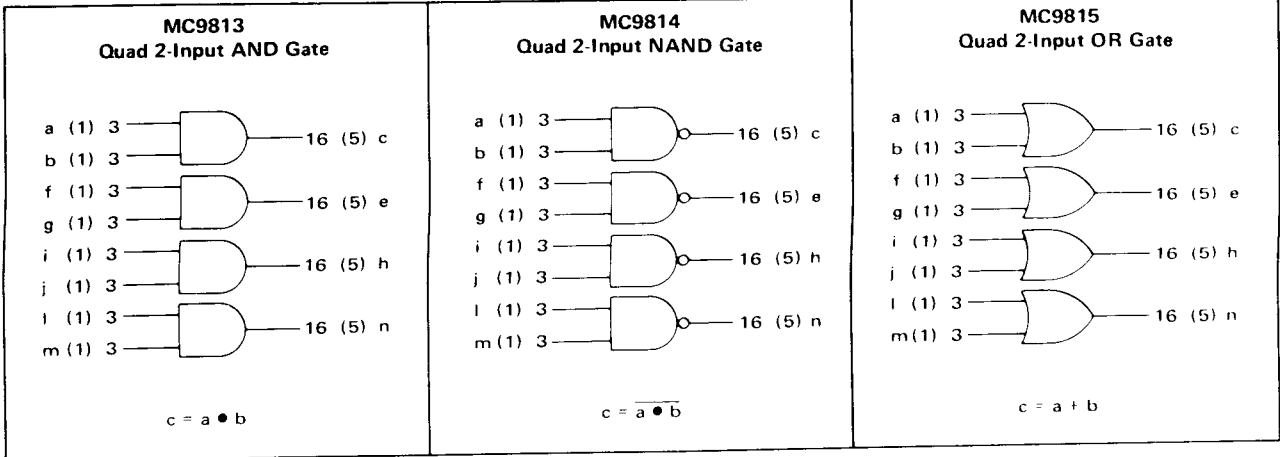
The numbers in parenthesis indicate loading factors for medium-power MRTL devices. The numbers at the end of the terminals indicate the normalized loading factors used for compatibility with the low-power mW MRTL devices when mixing the two power levels in a system. Pin numbers

vary with the package types. The alpha pin designations shown on the logic diagrams, used in conjunction with the Package Information Table (following the logic diagrams), make it possible to ascertain pin numbers for a specific device and package.

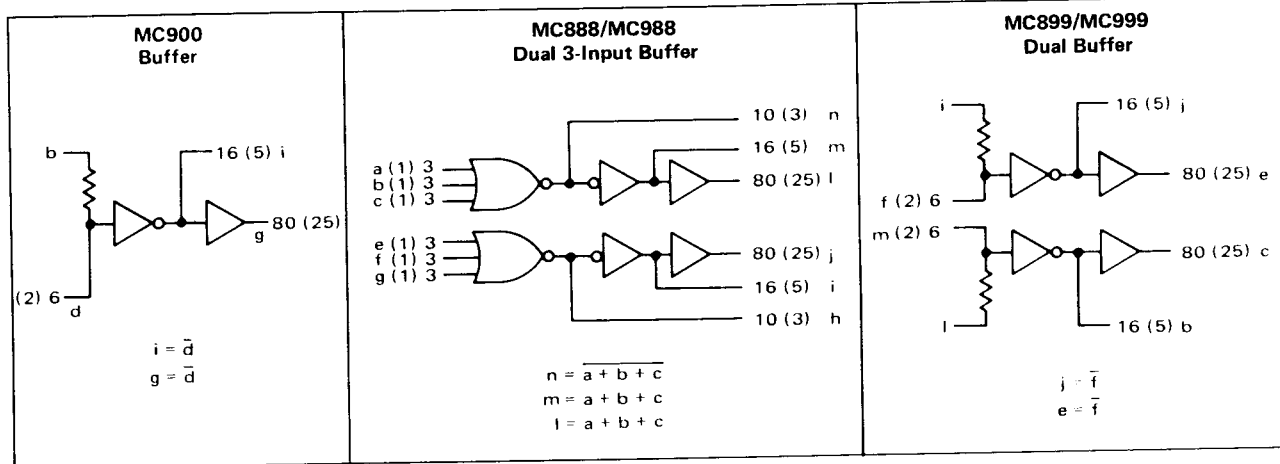
**GATES**



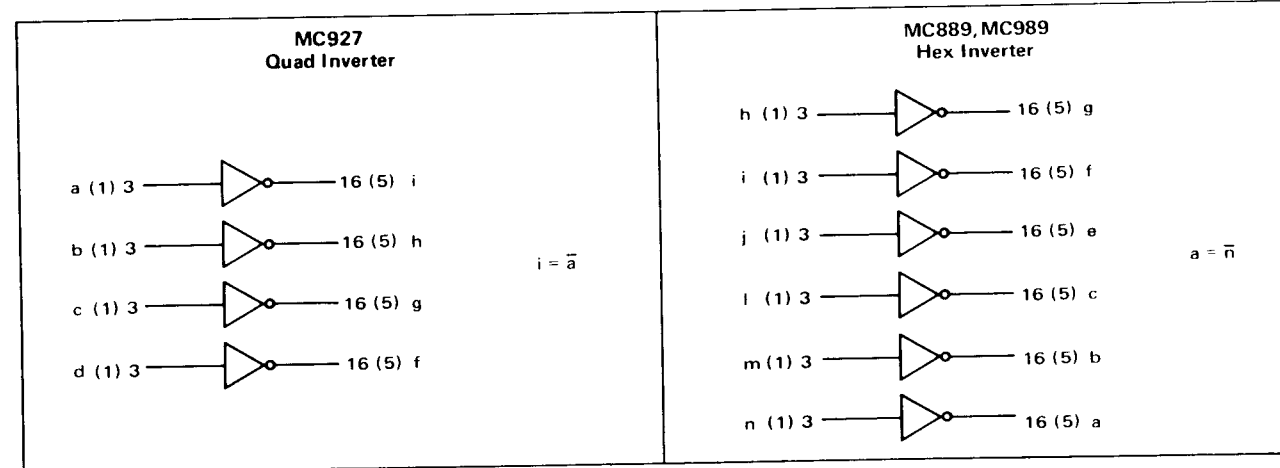
## GATES (continued)



## BUFFERS



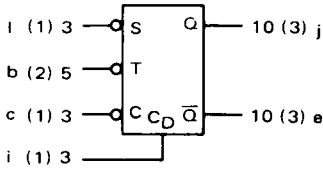
## INVERTERS



# MRTL LOGIC DIAGRAMS

## FLIP-FLOPS

**MC816, MC916**  
J-K Flip-Flop

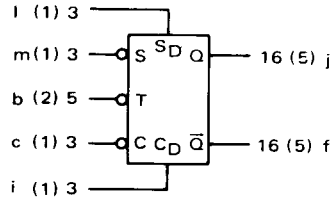


**CLOCKED INPUT OPERATION** ①

$t_n$ ②		$t_{n+1}$ ②	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

1. Direct input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

**MC826, MC926**  
J-K Flip-Flop



**CLOCKED INPUT OPERATION** ①

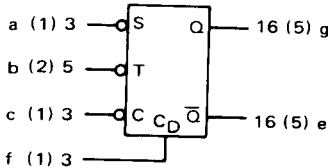
$t_n$ ②		$t_{n+1}$ ②	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

1. Direct inputs ( $C_D$  and  $S_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from  $S_D = C_D$  to  $S_D = C_D = 0$ . The output state cannot be pre-determined in the case where the input goes from  $S_D = C_D = 1$  to  $S_D = C_D = 0$ .

**DIRECT INPUT OPERATION**

$S_D$	$C_D$	Q	$\bar{Q}$
0	0	④	④
1	0	1	0
0	1	0	1
1	1	1	1

**MC974**  
J-K Flip-Flop



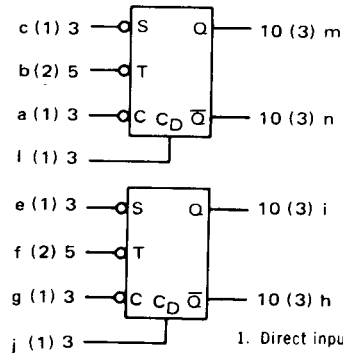
**CLOCKED INPUT OPERATION** ①

$t_n$ ②		$t_{n+1}$ ②	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

1. Direct input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

**NOTE:**  
Clock pulse fall time must be within the range of 10 ns to 100 ns on all J-K Flip-Flops except MC926, MC826F, and MC826G which have a range of 10 ns to 200 ns.

**MC890, MC990**  
Dual J-K Flip-Flop

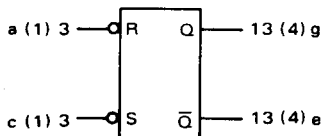


**CLOCKED INPUT OPERATION** ①  
(each Flip-Flop)

$t_n$ ②		$t_{n+1}$ ②	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

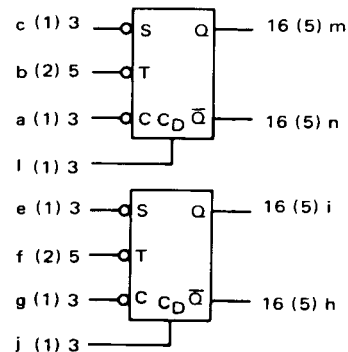
1. Direct input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

**MC902**  
R-S Flip-Flop



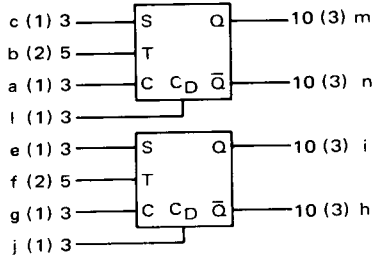
R	S	$Q_{n+1}$
0	0	$Q_n$
0	1	1
1	0	0
1	1	0

**MC891, MC991**  
Dual J-K Flip-Flop



## FLIP-FLOPS (continued)

**MC9802**  
Dual J-K Flip-Flop



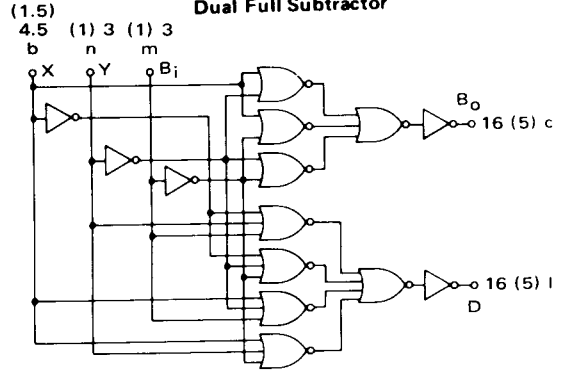
**CLOCKED INPUT OPERATION**

$t_n$ ②	$t_{n+1}$ ①	Q	$\bar{Q}$
1	1	$a_n$ ③	$\bar{a}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{a}_n$	$a_n$ ③

1. Preclear input ( $C_D$ ) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .
4. Clock pulse fall time must be <100 ns.

## FULL SUBTRACTOR

**MC897, MC997**  
Dual Full Subtractor



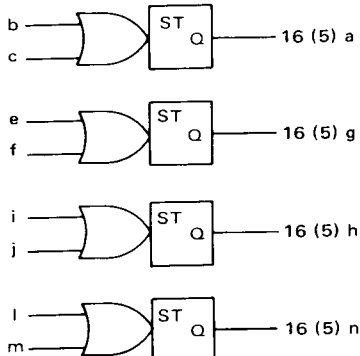
TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	$B_i$	D	$B_o$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = YXB_i + \bar{Y}X\bar{B}_i + Y\bar{X}\bar{B}_i + \bar{Y}\bar{X}B_i$$

$$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + Y\bar{X}B_i + YXB_i$$

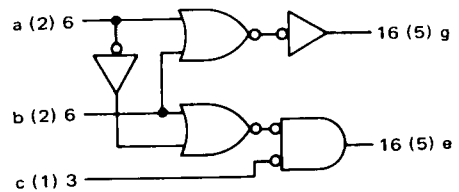
## SCHMITT TRIGGER

**MC9809**  
Quad Schmitt Trigger



## COUNTER ADAPTER

**MC901**  
Counter Adapter



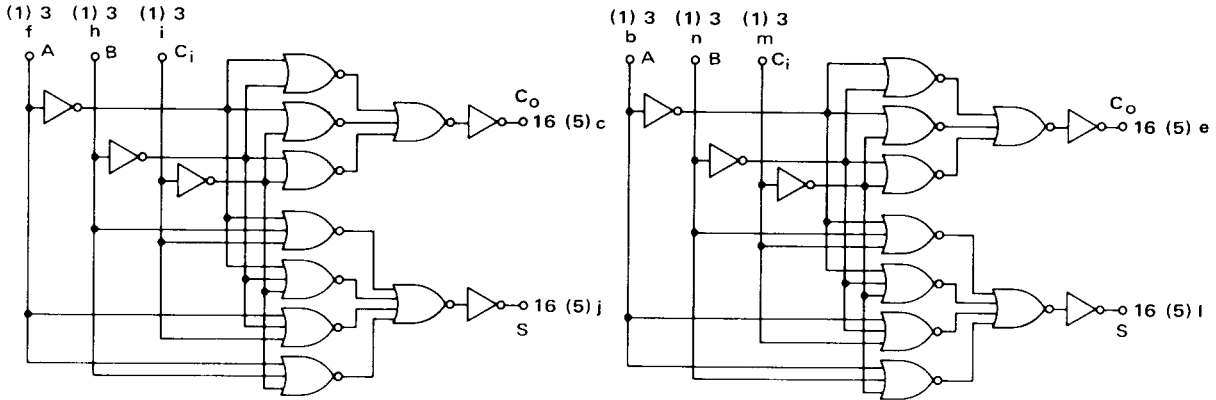
$$g = a + b$$

$$e = (\bar{a} + b) \bar{c}$$

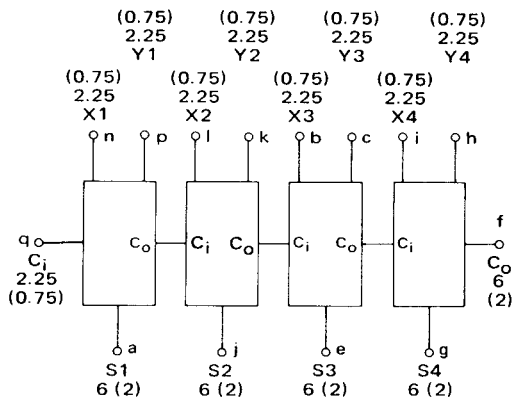
# MRTL LOGIC DIAGRAMS

## FULL ADDERS

**MC896, MC996  
Dual Full Adder**



**MC9804  
4-Bit Parallel Full Adder**



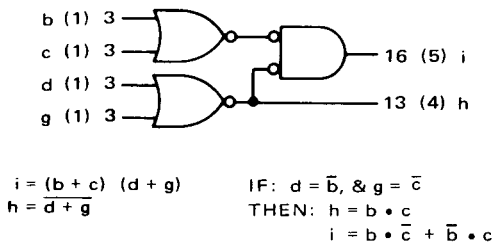
$$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$$

$$S = ABC_i + A\bar{B}\bar{C}_i + \bar{A}BC_i + \bar{A}\bar{B}\bar{C}_i$$

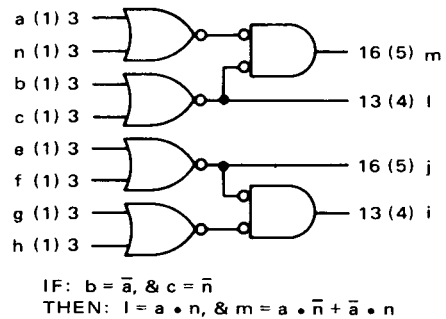
TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C <sub>i</sub>	S	C <sub>o</sub>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

## HALF ADDERS

**MC904  
Half Adder**

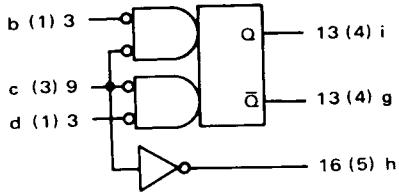


**MC875, MC975  
Dual Half Adder**



# SHIFT REGISTERS

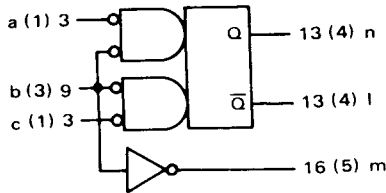
**MC905**  
Half-Shift Register



$$i = \bar{g} (b + c)$$

$$g = \bar{h} (c + d)$$

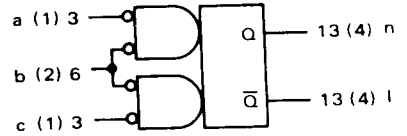
**MC883, MC983**  
Dual Half-Shift Register



$$n = \bar{l} (a + b)$$

$$l = \bar{m} (c + b)$$

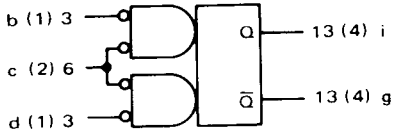
**MC884, MC984**  
Dual Half-Shift Register  
(without inverter)



$$n = \bar{l} (a + b)$$

$$l = \bar{m} (c + b)$$

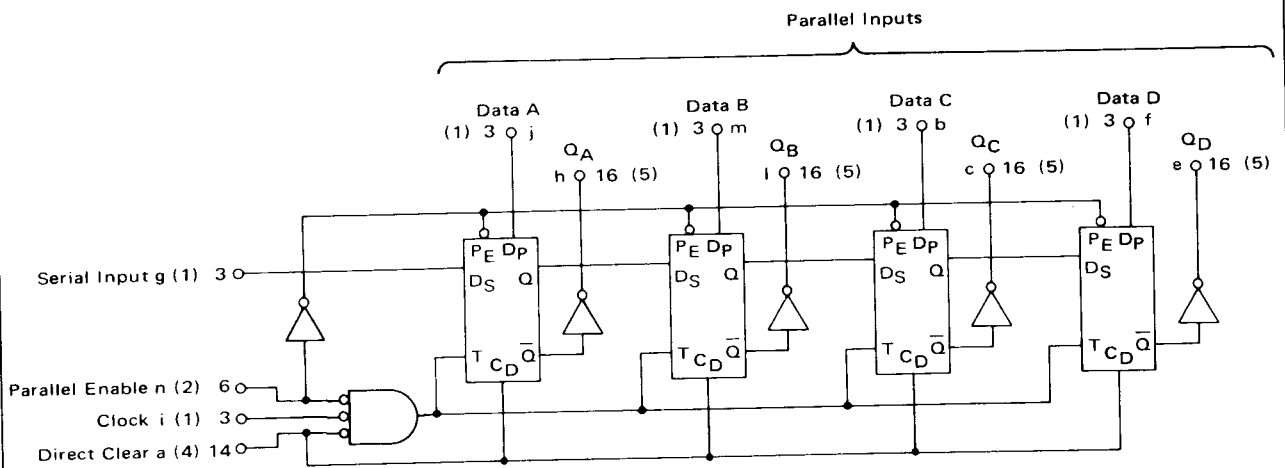
**MC906**  
Half-Shift Register  
(without inverter)



$$i = \bar{g} (b + c)$$

$$g = \bar{h} (c + d)$$

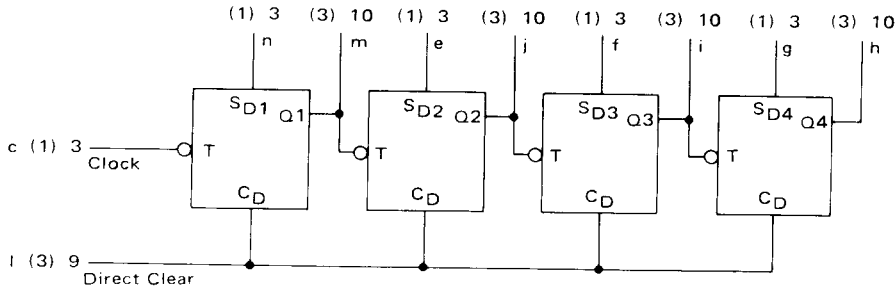
**MC894**  
Serial-Parallel Shift Register



# MRTL LOGIC DIAGRAMS

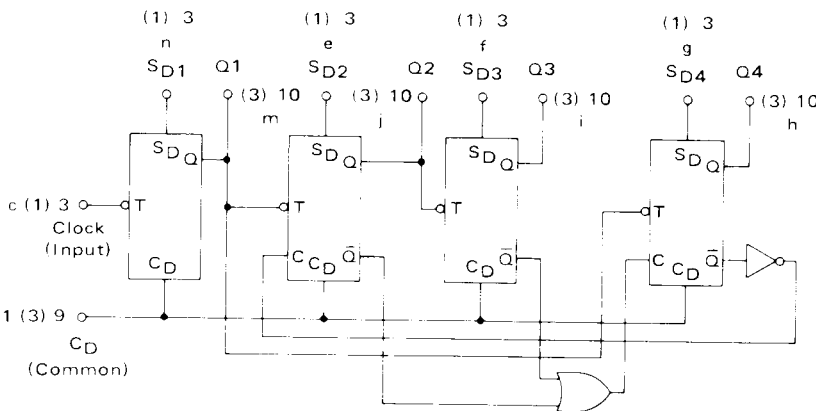
## COUNTERS

**MC877**  
Binary Up Counter



DECODING LOGIC	
0	$\bar{A} \bar{B} \bar{C} \bar{D}$
1	$A \bar{B} \bar{C} \bar{D}$
2	$\bar{A} B \bar{C} \bar{D}$
3	$A B \bar{C} \bar{D}$
4	$\bar{A} \bar{B} C \bar{D}$
5	$A \bar{B} C \bar{D}$
6	$\bar{A} B C \bar{D}$
7	$A B C \bar{D}$
8	$\bar{A} \bar{B} \bar{C} D$
9	$A \bar{B} \bar{C} D$
10	$\bar{A} B \bar{C} D$
11	$A B \bar{C} D$
12	$\bar{A} \bar{B} C D$
13	$A \bar{B} C D$
14	$\bar{A} B C D$
15	$A B C D$

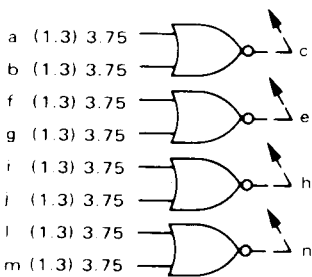
**MC880**  
Decade Up Counter



DECODING LOGIC				
0	$\bar{A}$	$\bar{B}$	$\bar{C}$	$\bar{D}$
1	A	$\bar{B}$	$\bar{C}$	$\bar{D}$
2	$\bar{A}$	B	$\bar{C}$	$\bar{D}$
3	A	B	$\bar{C}$	$\bar{D}$
4	$\bar{A}$	$\bar{B}$	C	$\bar{D}$
5	A	$\bar{B}$	C	$\bar{D}$
6	$\bar{A}$	B	C	$\bar{D}$
7	A	B	C	$\bar{D}$
8	$\bar{A}$	$\bar{B}$	C	D
9	A	$\bar{B}$	C	D

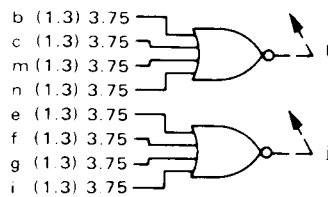
## EXPANDERS

**MC885, MC985**  
Quad 2-Input Expander



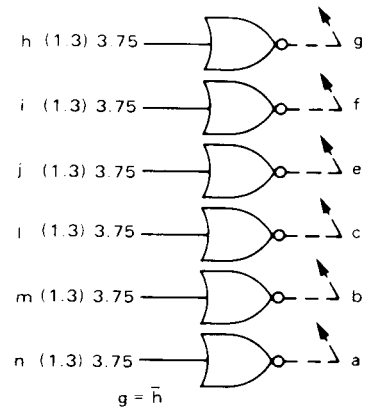
$c = \bar{a} + \bar{b}$

**MC886, MC986**  
Dual 4-Input Expander



$i = \bar{b} + \bar{c} + \bar{m} + \bar{n}$

**MC9819**  
Hex Expander

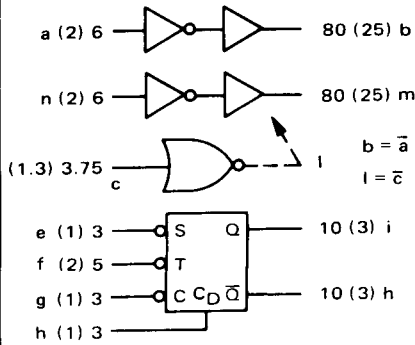


$g = \bar{h}$



## MULTIFUNCTION DEVICES

**MC879**  
(1 J-K Flip-Flop, 1 Expander, 2 Buffers)



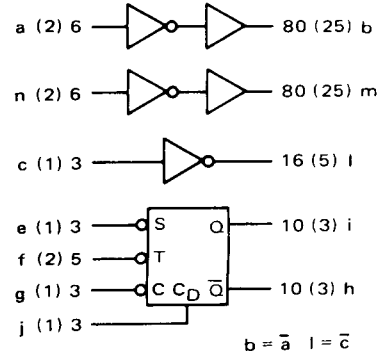
**CLOCKED INPUT OPERATION<sup>①</sup>**

$t_n$ ②		$t_{n+1}$ ③	
S	C	Q	$\bar{Q}$
1	1	$Q_n$ ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	$Q_n$ ③

1. Direct input (C<sub>D</sub>) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted  $t_n$  and the time period subsequent to this transition is denoted  $t_{n+1}$ .
3.  $Q_n$  is the state of the Q output in the time period  $t_n$ .

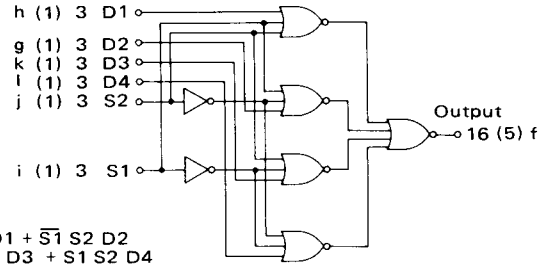
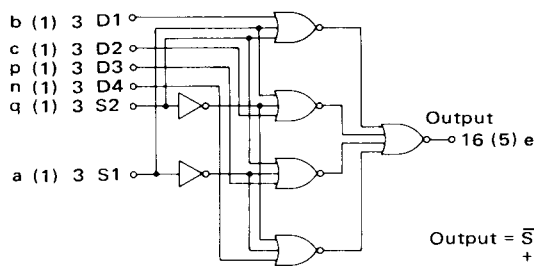
**MC887**

(1 J-K Flip-Flop, 1 Inverter, 2 Buffers)



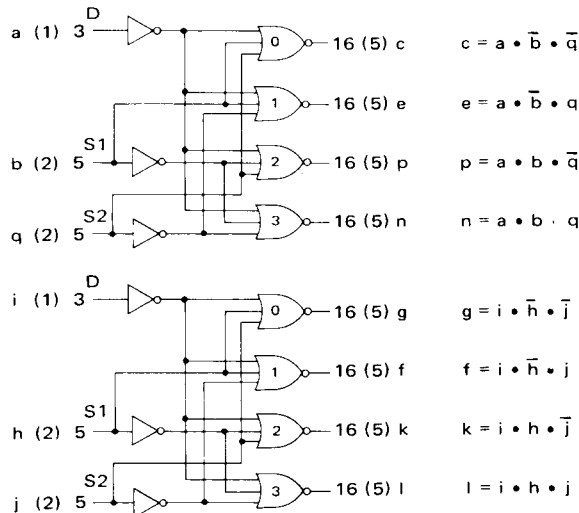
## DATA ROUTING FUNCTIONS

**MC9801**  
Dual 4-Channel Data Selector



$$\text{Output} = \bar{S}_1 \bar{S}_2 D_1 + \bar{S}_1 S_2 D_2 + S_1 \bar{S}_2 D_3 + S_1 S_2 D_4$$

**MC9807**  
Dual 4-Channel Data Distributor



**TRUTH TABLE**

Input Select		Data Line Selected
S1	S2	
0	0	D1
0	1	D2
1	0	D3
1	1	D4

**TRUTH TABLE**

Pin Numbers	INPUTS			OUTPUTS								
	D	S1	S2	0	1	2	3					
a	i	b	h	q	j	c	f	e	p	k	n	l
Level	0	*	*	0	0	0	0	0	0	0	0	0
	1	0	0	1	0	0	0	0	0	0	0	0
	1	0	1	0	1	0	0	0	0	0	0	0
	1	1	0	0	0	1	0	0	0	0	0	0
	1	1	1	0	0	0	0	0	0	0	0	1

\* Either state.

# MRTL LOGIC DIAGRAMS

## MAXIMUM RATINGS ( $T_A = 25^{\circ}\text{C}$ )

Rating	Symbol	Value	Unit
Input Voltage	—	+4	Vdc
Power Supply Voltage (Pulsed $\leq 1$ second)	—	+6	Vdc
Operating Temperature Range MC900 Series	$T_A$	-55 to +125	$^{\circ}\text{C}$
MC800P Series		0 to +75	
Storage Temperature Range Metal Can, Flat Package Plastic Package	$T_{\text{stg}}$	-65 to +150	$^{\circ}\text{C}$
		-55 to +125	

## INSTRUCTIONS FOR USE OF PACKAGE INFORMATION TABLE

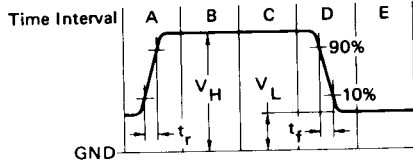
MC900 and MC800 Series Medium-Power MRTL devices are available in the packages pictured in the following table as indicated on the line following each device type number. Plastic and dual-in-line ceramic packaged devices are available in the MC800 Series only.

Pin numbers for any of the following devices and packages may be determined by:

- Find the device among the logic diagrams appearing on the preceding pages (grouped by function). Note the alpha pin designations for the device.
- Find the device type number in the left hand columns of the "Package Information Table".
- The letters in the columns following the type number and below the drawing of the desired package indicate the correct pin numbers for the specific package by their numbered positions beneath the package drawing. (These letters are the same as indicated on the logic diagram for the device.)
- Notes: Blanks in an area following the type number and directly beneath a package indicate the device is not available in that package. A dash indicates this pin or lead is not connected nor otherwise utilized for this device and package.  
\* indicates this pin number is the ground connection for this device and package.  
# indicates this pin number is the  $V_{CC}$  connection for this device and package.

## TYPICAL OPERATING CHARACTERISTICS FOR mW MRTL J-K FLIP-FLOPS

**FIGURE 1 - CLOCK PULSE DEFINITION**



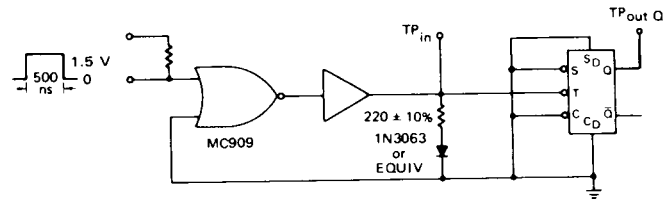
SEQUENCE OF EVENTS:

- A. Voltage applied to Clock pin is raised to  $V_H$ .  $t_r$  is not critical but should be  $< 1.0 \mu s$ .
- B. Biases of all other inputs are applied.  $V_{CC}$  is applied without interruption throughout the testing.
- C. Apply momentary ground, when applicable.
- D. Clock pulse is allowed to fall to  $V_L$ .  $t_f$  remains within 10 ns minimum and 100 ns maximum.
- E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC800 Series

$T_A$	$V_L$	$V_H$
+25°C	+460 ± 2.0 mVdc	+850 ± 2.0 mVdc
0°C	+500 ± 2.0 mVdc	+900 ± 2.0 mVdc
+75°C	+400 ± 2.0 mVdc	+760 ± 2.0 mVdc

**FIGURE 2 - TOGGLE MODE TEST CIRCUIT**



$f = 4.0 \text{ MHz}$   
 Duty Cycle = 25% to 75%  
 $t_r$  &  $t_f < 10 \text{ ns}$

NOTE:

Waveform at the output test point should be ½ the frequency of the waveform at the input test point.

MC900 Series

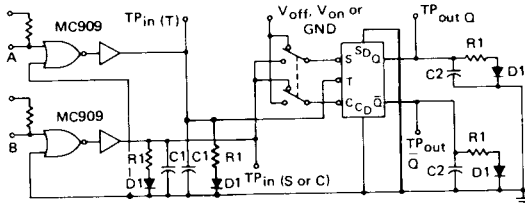
$T_A$	$V_L$	$V_H$
+25°C	+450 ± 2.0 mVdc	+800 ± 2.0 mVdc
-55°C	+650 ± 2.0 mVdc	+985 ± 2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+605 ± 2.0 mVdc

**SWITCHING TIMES**

Test	Figure No. 3	Maximum (ns)
$t_{T-Q-}$	3B	150
$t_{T-Q+}$	3B	150
$t_{T-Q-}$	3B	100
$t_{T-Q+}$	3B	100
$t_{S+T-}$	3C	50
$t_{S-T-}$	3C	30
$t_{C+T-}$	3C	50
$t_{C-T-}$	3C	30
$t_{T-S+}$	3C	0
$t_{T-S-}$	3C	+5
$t_{T-C+}$	3C	0
$t_{T-C-}$	3C	+5
$t_{C_D+Q-}$	4	140
$t_{C_D+Q+}$	4	70
$t_{S_D+Q+}$	4	70
$t_{S_D+Q-}$	4	140

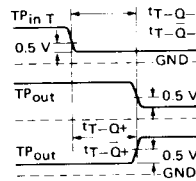
### SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS

**FIGURE 3A - SET-UP, RELEASE AND SWITCHING TIMES TEST CIRCUIT**



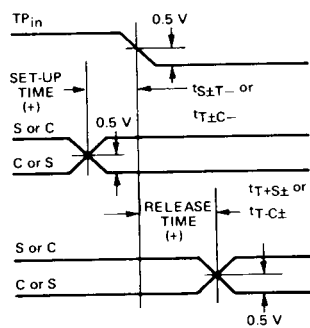
$C1 = 20 \text{ pF}$  Including Jig and Probe       $R1 = 1.5 \text{ k ohms} \pm 1.0\%$   
 $C2 = 8.0 \text{ pF}$  Including Jig and Probe       $D1 = 1N3063$  or Equivalent

**FIGURE 3B - SWITCHING TIME WAVEFORMS**



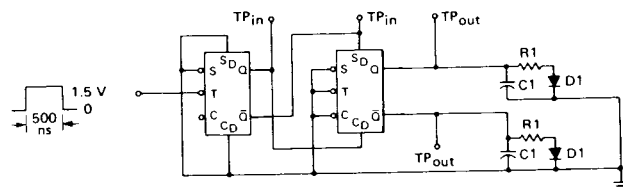
NOTE: Whichever input pin (S or C) is tied to MC909 Buffer on input pin B is at virtual ground when the input is tied to  $V_{BOT}$ .

**FIGURE 3C - SET-UP AND RELEASE TIME**



FOR DEFINITIONS OF SET-UP AND RELEASE TIMES, SEE GENERAL INFORMATION SECTION.

**FIGURE 4 - DIRECT SET AND DIRECT CLEAR PROPAGATION DELAY TIME**



$f = 1.0 \text{ MHz}$   
 $t_r$  &  $t_f < 10 \text{ ns}$

$C1 = 8.0 \text{ pF}$  Including Jig and Probe  
 $R1 = 1.5 \text{ k ohms} \pm 1.0\%$   
 $D1 = 1N3063$  or EQUIVALENT

